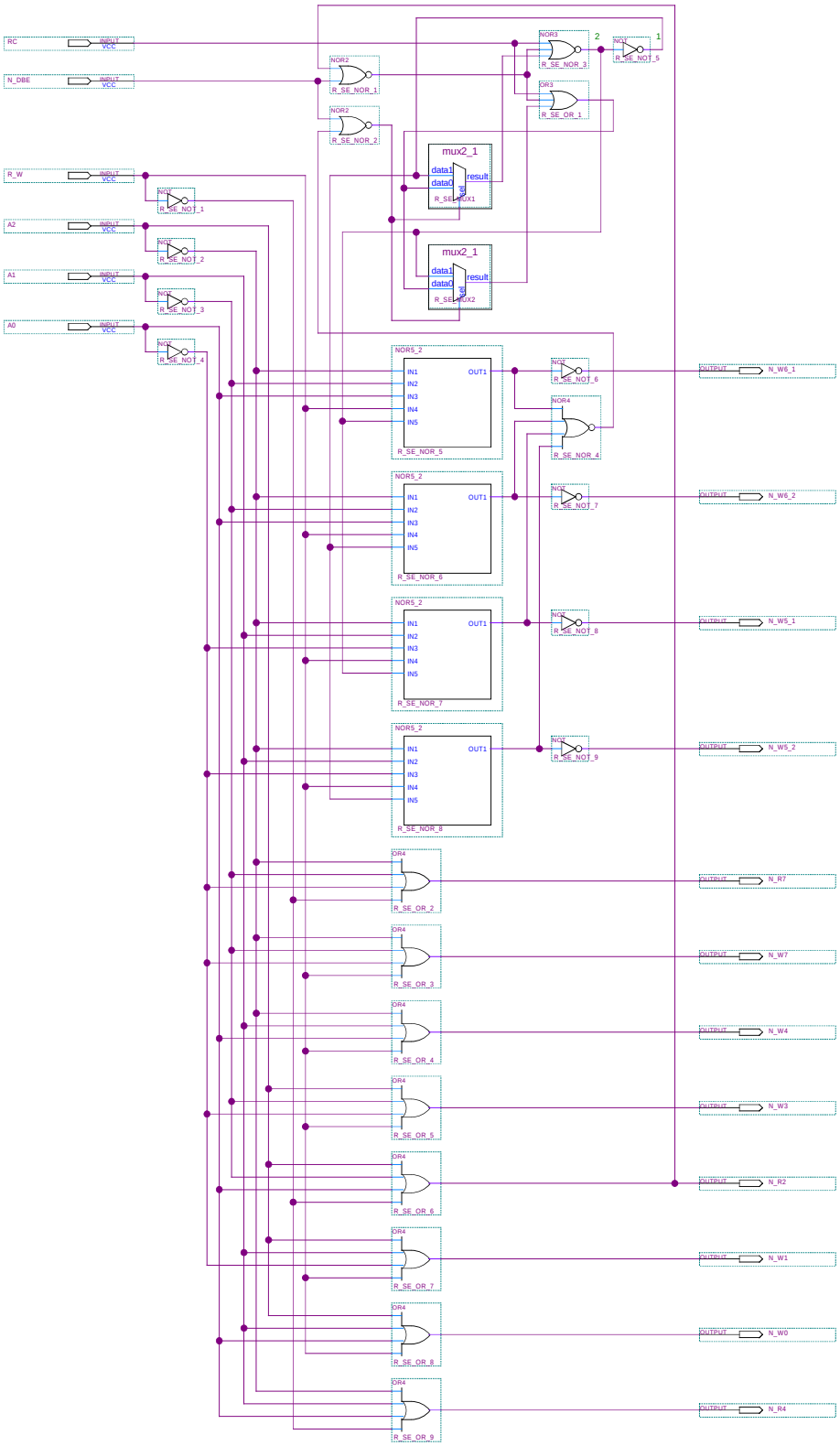
RC
N_DBE
R_W
A2
A1
A0
INPUT
VCC
NOR2
R_SE_NOR_1
R_SE_NOR_2
NOR3
R_SE_NOR_3
R_SE_NOT_5
OR3
R_SE_OR_1
mux2_1
data1
data0
result
sel
R_SE_MUX1
R_SE_MUX2
NOT
R_SE_NOT_1
R_SE_NOT_2
R_SE_NOT_3
R_SE_NOT_4
R_SE_NOT_6
R_SE_NOT_7
R_SE_NOT_8
R_SE_NOT_9
NOR5_2
IN1
IN2
IN3
IN4
IN5
OUT1
R_SE_NOR_5
R_SE_NOR_6
R_SE_NOR_7
R_SE_NOR_8
NOR4
R_SE_NOR_4
OR4
R_SE_OR_2
R_SE_OR_3
R_SE_OR_4
R_SE_OR_5
R_SE_OR_6
R_SE_OR_7
R_SE_OR_8
R_SE_OR_9
OUTPUT
N_W6_1
N_W6_2
N_W5_1
N_W5_2
N_R7
N_W7
N_W4
N_W3
N_R2
N_W1
N_W0
N_R4